

Preliminary DATA SHEET

CFORTH-QSFP28-100G-SR4
100G QSFP28 SR4 Transceiver

CFORTH-QSFP28-100G-SR4 Overview

CFORTH-QSFP28-100G-SR4 QSFP28 SR4 optical transceivers are based on Ethernet IEEE 802.3bm standard standard. QSFP28 SR4 offers 4 independent transmit and receive channels, each capable of 25G for an aggregate bandwidth of 100G.

Product Features

- 4x25Gbps 850nm
- Up to 103.1Gbps
- QSFP28 MSA compliant
- Up to 70m OM3 or 100m OM4 Multimode Fiber.
- Reliable VCSEL array technology
- Single 1X12 MPO receptacle
- RoHS Compliance
- Operating temperature range: 0°C to 70°C.

Applications

- 100GBASE-SR4 100G Ethernet

Ordering Information

<i>Part Number</i>	<i>Description</i>
CFORTH-QSFP28-100G-SR4	100G QSFP28 850nm MPO Connectors, Up to 70m(OM3) or 100m(OM4) on MMF

General Specifications

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Remarks</i>
Bit Error Rate	BER			10^{-12}		
Operating Temperature	T_{OP}	0		70	°C	Case temperature
Storage Temperature	T_{STO}	- 40		85	°C	Ambient temperature
Input Voltage	V_{CC}	3.13	3.3	3.46	V	
Maximum Voltage	V_{MAX}	- 0.5		3.6	V	For electrical power interface

Optical Characteristic – Transmitter

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Remarks</i>
Average Launch Power (per lane)	P	- 8.4		2.4	dBm	
Optical Center Wavelength	λ_C	840		860	nm	
Extinction Ratio	ER	3			dB	
RMS Spectral Width	$\Delta\lambda$			0.65	nm	
Relative Intensity Noise	RIN			- 128	dB/Hz	
Transmitter Dispersion Penalty	TDP			3.5	dB	
Transmitter Eye Mask						Compliant with IEEE 802.3bm
Launch Power of OFF Transmitter	P_{OUT_OFF}			- 30	dBm	Average

Optical Characteristics – Receiver

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Remarks</i>
Optical Center Wavelength	λ_C	840		860	nm	
Optical Input Power (per lane)	P_{IN}	-10.3		2.4	dBm	Average, Informative
Damage Threshold	P	3.3			dBm	
Stressed Receiver Sensitivity in OMA, per lane				-5.2	dBm	
Receiver Reflectance	TR_{RX}			- 12	dB	
LOS Assert	LOS_A	-25			dBm	
LOS De-Assert	LOS_D			-13	dBm	
LOS Hysteresis		0.5			dB	

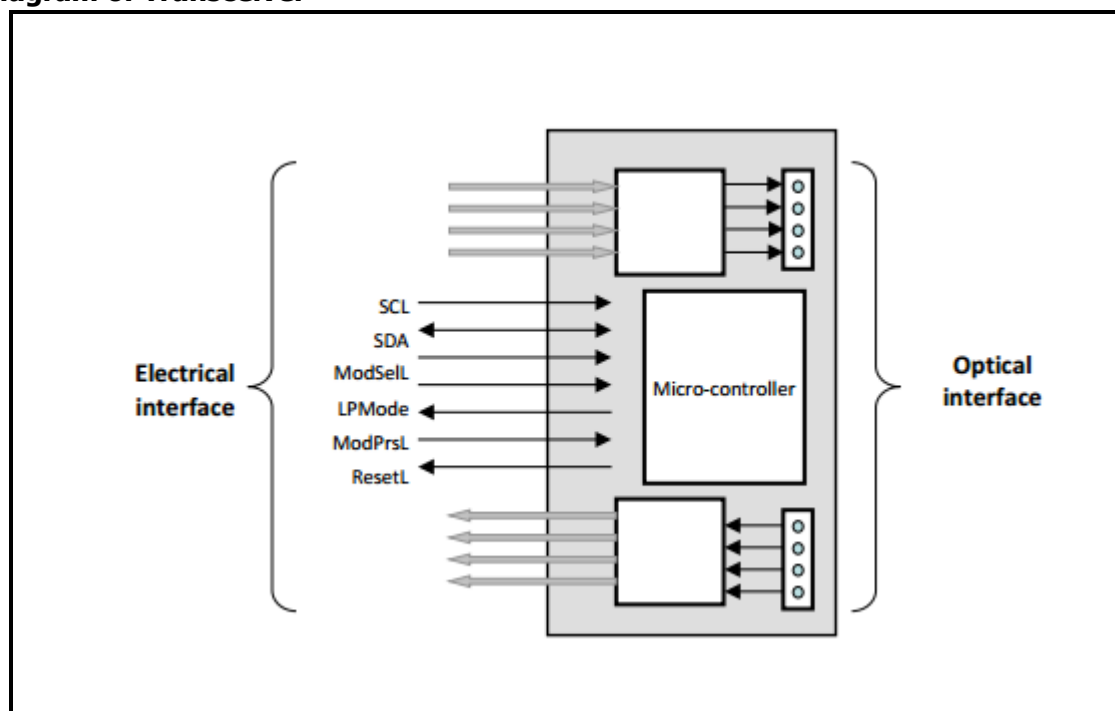
Electrical Characteristics – Transmitter

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Remarks</i>
Data Rate Per Channel	Dr		25.78125		GB/s	
Differential Input Amplitude	V_{IN_PP}	300		1200	mV	
Transmit disable voltage	V_D	$V_{CC}-1.3$		V_{CC}	V	
Transmit enable voltage	V_{EN}	V_{EE}		$V_{EE}+0.8$	V	

Electrical Characteristics – Receiver

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Remarks</i>
Data Rate Per Channel	D_r		25.78125		GB/s	
Differential Output Amplitude	V_{out_PP}	340		700	mV	
Differential Output Amplitude in Squelched state	V_{out_sq}			50	mV	
Single Ended Voltage Tolerance	V	-0.3		3.8	V	
Output AC Common Mode Voltage	V_{cm}			7.5	mV	RMS
Output Transition Time	T_r, T_f	28			ps	
Total Jitter	T_j			0.7	UIp-p	
Deterministic Jitter	DJ			0.4	UIp-p	
Eye Mask						See note

Block Diagram of Transceiver



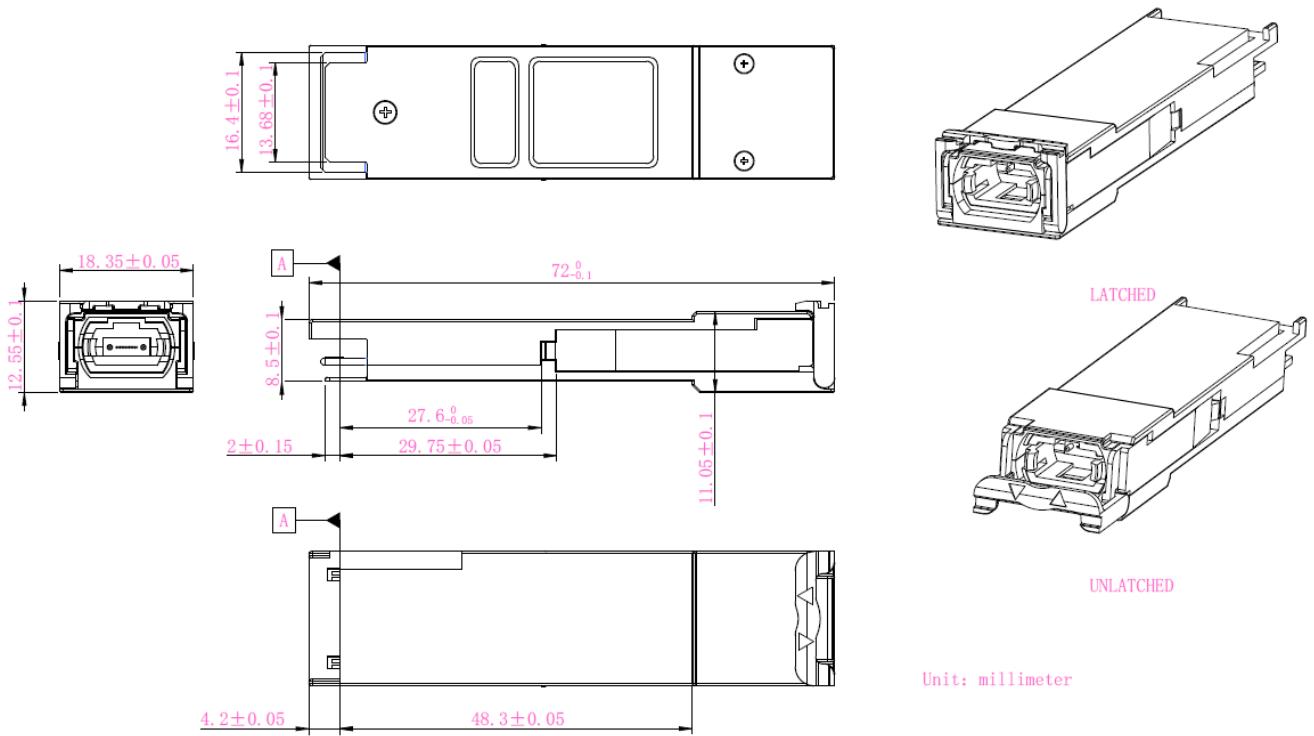
The QSFP28-SR4 has miniature optical engine embedded into QSFP28 module. The engines interconnect 4 independent transmit/receive lanes.

A functional block diagram of the engine is shown in the above Figure. The transmitter sections consists of a 4-channel VCSEL array, a 4-channel input buffer and laser driver.

An on board micro-controller provides control, diagnostic and monitoring for the cable functions, as well as the external I2C serial communication interface.

The Receiver section consists of a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4-channel output buffer.

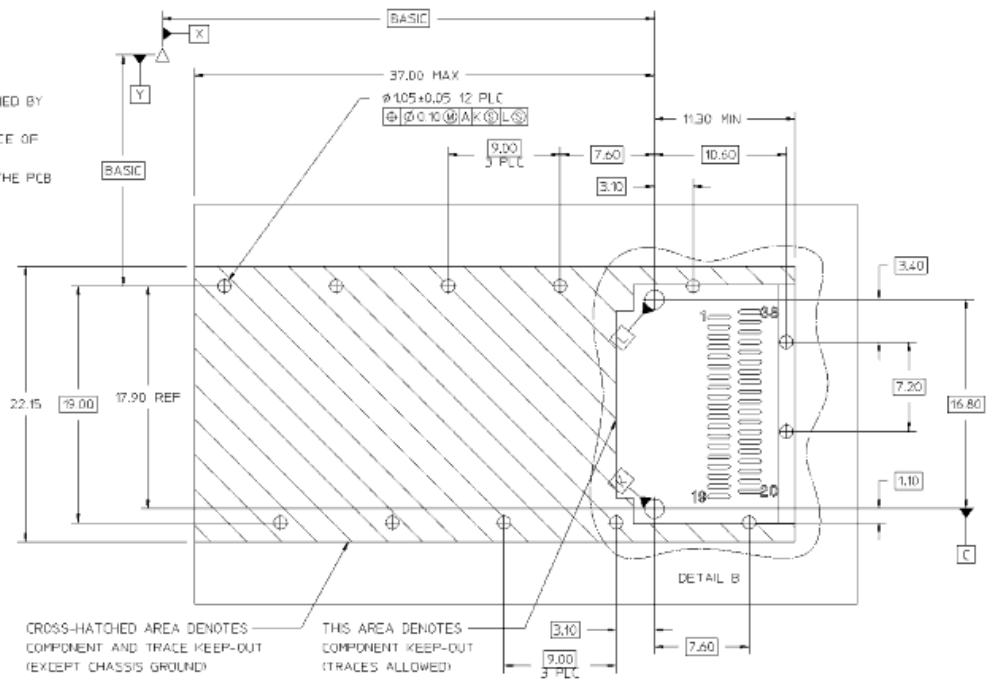
Dimensions

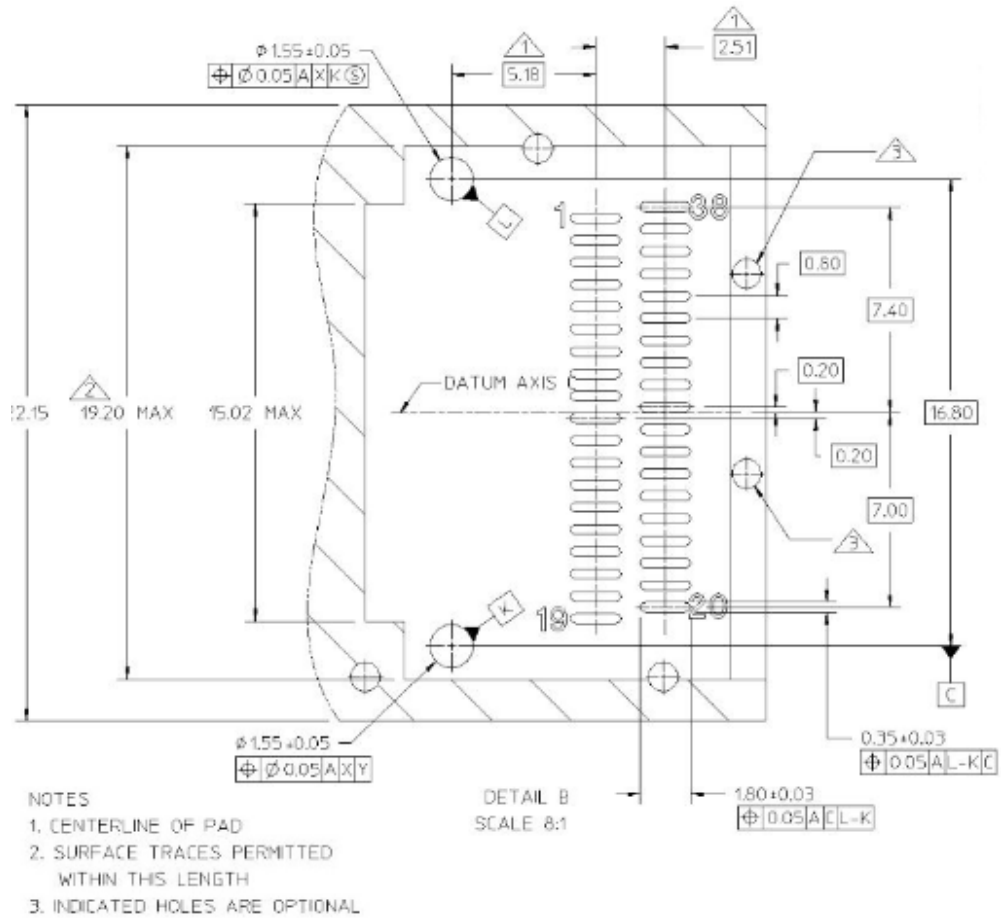


**ALL DIMENSIONS ARE ±0.2mm UNLESS OTHERWISE SPECIFIED
UNIT: mm**

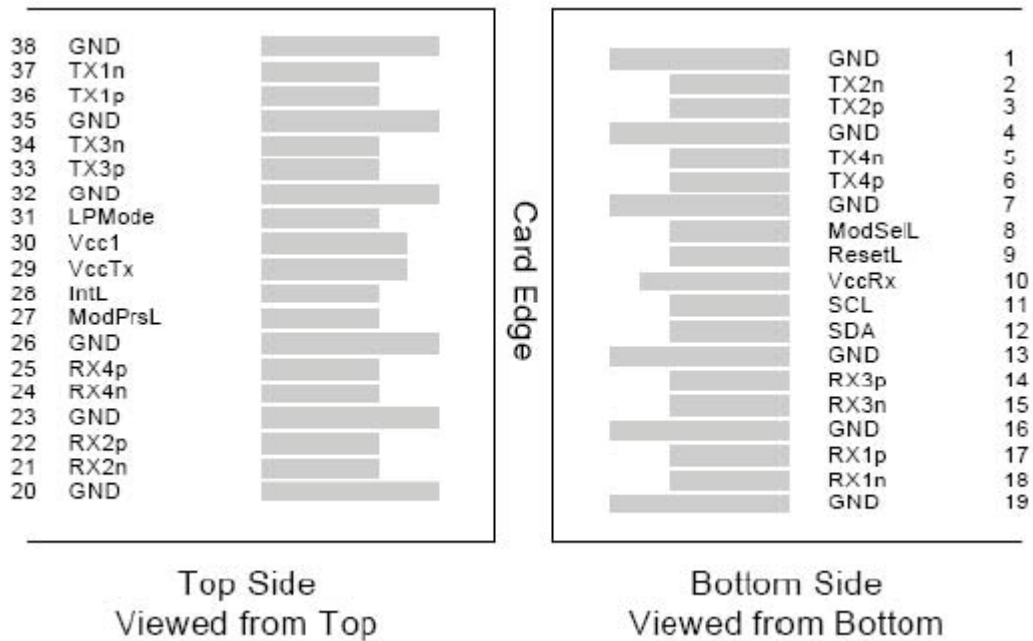
PCB Layout Recommendation

- NOTES
1. DATUM X & Y ARE ESTABLISHED BY THE CUSTOMER'S FIDUCIAL
 2. DATUM A IS THE TOP SURFACE OF THE HOST BOARD
 3. LOCATION OF THE EDGE OF THE PCB IS APPLICATION SPECIFIC
 4. FINISHED PTH HOLE SIZE





Electrical Pad Layout



Pin Assignment

<i>PIN #</i>	<i>Symbol</i>	<i>Description</i>	<i>Remarks</i>
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	V _{cc} RX	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	V _{cc} TX	+3.3V Power Supply transmitter	
30	V _{cc1}	+3.3V Power Supply	
31	LPMODE	Low Power Mode	
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	

References

1. IEEE standard 802.3bm. IEEE Standard Department.
2. QSFP28 4X PLUGGABLE TRANSCEIVER – SFF-8665